IN THE SPECIFICATION

Please amend the specification as follows:

On page 5, the paragraph starting at line 25

Referring still to Fig. 1, logic level shift circuit 120 receives a master VREF_CONTROL signal at its input 122 from a logic device core ~~(not shown)~~ and the dedicated supply signal VCC_DED. logic level shift circuit 130 receives an inverted or complementary version of the VREF_CONTROL signal at its input 132 and the I/O supply signal VCC_IO. In the illustrated embodiment, VREF_CONTROL is provided to input 132 via an inverter 125, but, alternatively, a complementary control signal may be generated in the logic core and then provided directly to circuit 130. As shown, the level-shifted control signal at the output 124 of logic level shift circuit 120 is provided to the gates of NMOS transistors T1 and T2 and PMOS transistor T5. The level-shifted control signal at the output 134 of circuit 130 is provided to the gates of PMOS transistors T3 and T4 and the gate of NMOS transistor T6.